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CARBON CONTAINING SILICON OXIDE FILM HAVING HIGH ASHING TOLERANCE AND ADHESION

Field of the Invention

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The present invention relates generally to an insulating film having a low dielectric constant, and more particularly to an insulating film having a low dielectric constant which is used, for example, as an interlayer insulating film of a semiconductor device.

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Background of the Invention

Recently, according to an increase in demand for higher integration degree of a semiconductor device, a multi-layer wiring technology has become of much note. In the multi-layer wiring structure, a bottleneck against high speed operation of elements is capacitance between wires. In order to decrease the capacitance between wires, it is necessary to reduce the dielectric constant (or relative dielectric constant) of an interlayer insulating film.

Conventionally, a silicon dioxide (SiO₂) film is generally used. Recently, however, other insulating film materials having lower dielectric constant are energetically developed.

The conventional silicon dioxide film is formed by adding oxygen O₂ or nitrous oxide N₂O as oxidizing agent to material gas such as SiH₄, Si(OC₂H₅)₄ and the like, and by using a plasma enhanced CVD method and the like. The dielectric constant of silicon dioxide obtained in this way is approximately 4.0. On the other hand, it is reported that a

carbon containing silicon oxide (SiOCH) film, which is formed by using methyl silane based precursor (for example, trimethyl silane or tetramethyl silane) as material gas and which is formed by using a plasma enhanced CVD method, has the 5 dielectric constant of 3 or lower. In the SiOCH film, CH₃ group as an end group is introduced into -O-Si-O- network, thereby reducing the density to decrease the dielectric constant thereof. For example, see page 3, column 2 through page 4, column 4 of the specification of U.S. Patent No. 6,159,871, and 10 page 11, column 4 through page 16, column 14 of the specification of U.S. Patent No. 6,054,879.

However, the CH₃ groups contained in the SiOCH film are often destructed in the O₂ ashing process when trenches and vias are formed in the film. Therefore, the SiOCH film is 15 susceptible to deterioration of film quality such as film contraction, moisture absorption and the like. This is because, the CH₃ group is located in the end portion of the -O-Si-O- network, and easily reacts with O ions and radicals in the ashing atmosphere.

20 At present, in developing next generation devices, an effort is energetically performed to further reduce the dielectric constant by making the SiOCH film porous. However, when the SiOCH film becomes porous, the above-mentioned ashing damage becomes prominent. Also, in the via-first method 25 which is most typical among the dual-damascene processes for forming wiring structure, side walls of the through holes (vias) formed in the process of the method are exposed to the ashing processes twice when the vias are formed and when the trenches are formed. When the side walls of the vias are 30 deteriorated due to the ashing damage and moisture absorption

becomes large, deterioration of yield of vias becomes large.

Further, when the SiOCH film is patterned, an SiO₂ film (CAP-SiO₂ film) is formed on the SiOCH film as a mask for patterning. However, adhesion of the SiOCH film with the

5 CAP-SiO₂ film is lower than that of the conventional film such as an SiO₂ film, an SiON film, an SiN film, an HSQ film and the like. This is because, the CH₃ groups contained in the film is hydrophobic, and affinity thereof with the SiO₂ film is relatively low.

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Summary of the Invention

Therefore, it is an object of the present invention to provide an insulating film which can be used as an interlayer insulating film of a semiconductor device and in which ashing tolerance of the insulating film can be improved without causing a rise in dielectric constant of the insulating film.

15 It is another object of the present invention to provide an insulating film which can be used as an interlayer insulating film of a semiconductor device and which has improved adhesion with an SiO₂ film.

20 It is still another object of the present invention to provide a semiconductor device having an interlayer insulating film in which ashing tolerance of the interlayer insulating film can be improved without causing a rise in dielectric constant of the insulating film.

25 It is still another object of the present invention to provide a semiconductor device having an interlayer insulating film in which the interlayer insulating film has improved adhesion with an SiO₂ film.

It is still another object of the present invention to obviate the disadvantages of the conventional insulating film and the semiconductor device using the conventional insulating film.

5 According to an aspect of the present invention, there is provided an insulating film comprising a carbon containing silicon oxide (SiOCH) film which has Si-CH₂ bond in the carbon containing silicon oxide film.

According to another aspect of the present invention, 10 there is provided a semiconductor device having an interlayer insulating film formed on or over a semiconductor substrate and a metal wiring conductor which is formed by filling a wiring trench formed in the interlayer insulating film with Cu containing metal via a barrier metal, wherein the interlayer 15 insulating film includes the insulating film comprising a carbon containing silicon oxide (SiOCH) film which has Si-CH₂ bond in the carbon containing silicon oxide film.

According to still another aspect of the present invention, there is provided a semiconductor device having an interlayer 20 insulating film formed on or over a semiconductor substrate, an opening which is formed in the interlayer insulating film and which reaches a lower layer metal wiring conductor, and a metal plug which is formed by filling the opening with Cu containing metal via a barrier metal, wherein the interlayer 25 insulating film includes the insulating film comprising a carbon containing silicon oxide (SiOCH) film which has Si-CH₂ bond in the carbon containing silicon oxide film.

According to still another aspect of the present invention, there is provided a semiconductor device having an interlayer 30 insulating film formed on or over a semiconductor substrate, a

wiring trench formed in the interlayer insulating film, an opening which is formed in the interlayer insulating film and which reaches a lower layer metal wiring conductor from the bottom portion of the wiring trench, and a metal wiring

5 conductor and metal plug which are formed by filling the wiring trench and the opening with Cu containing metal via a barrier metal, wherein the interlayer insulating film includes the insulating film comprising a carbon containing silicon oxide (SiOCH) film which has Si-CH₂ bond in the carbon containing

10 silicon oxide film.

In the above, it is preferable that the proportion of Si-CH₂ bond (1360cm⁻¹) to Si-CH₃ bond (1270cm⁻¹) in the insulating film is in a range from 0.03 to 0.05 measured as a peak height ratio of FTIR spectrum.

15 It is also preferable that the relative dielectric constant of the insulating film is equal to or lower than 3.1.

It is further preferable that the carbon containing silicon oxide (SiOCH) film is formed by using plasma enhanced CVD process.

20 It is advantageous that the carbon containing silicon oxide (SiOCH) film comprises methylsilsesquioxane.

It is also advantageous that, as a portion of the interlayer insulating film, an SiO₂ film is formed on the upper layer portion of the insulating film.

25 It is further advantageous that, as a portion of the interlayer insulating film, an insulating film for preventing metal diffusion is formed on the lower layer portion of the insulating film.

30 It is preferable that the Cu containing metal contains, in addition to Cu, at least one of Si, Al, Ag, W, Mg, Be, Zn, Pd, Cd,

Au, Hg, Pt, Zr, Ti, Sn, Ni and Fe.

Brief Description of the Drawings

5 These and other features, and advantages, of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which like reference numerals designate identical or corresponding parts throughout the
10 figures, and in which:

Fig. 1 is a schematic view illustrating a plasma enhanced CVD system used for forming an insulating film according to the present invention;

15 Fig. 2A is a graph showing the RF power dependence of FT-IR characteristics of insulating films according to the present invention, and especially showing peak curves of Si-CH₂ in FT-IR spectra of SiOCH films formed in various RF power conditions;

20 Fig. 2B is a graph showing the RF power dependence of FT-IR characteristics of insulating films according to the present invention, and especially showing peak curves of Si-CH₃ in FT-IR spectra of SiOCH films formed in various RF power conditions;

25 Fig. 2C is a table showing ratios of Si-CH₂ to Si-CH₃ of SiOCH films formed in various RF power conditions;

Fig. 3 is a graph showing relationships between Si-CH₂/Si-CH₃ bond ratio and relative dielectric constant, and between Si-CH₂/Si-CH₃ bond ratio and a rise in dielectric constant caused by ashing, in an insulating film according to
30 the present invention;

Fig. 4 is a graph showing a relationship between Si-CH₂/Si-CH₃ bond ratio and adhesion, in an insulating film according to the present invention;

5 Fig. 5 is an illustration showing relationships between parameters concerning various film forming conditions and Si-CH₂/Si-CH₃ bond ratio;

Fig. 6 is a cross sectional view showing a semiconductor device according to an embodiment of the present invention;

10 Figs. 7A-7D are cross sectional views illustrating in order a process of forming the semiconductor device shown in Fig. 6;

15 Fig. 8 is a graph showing a relationship between Si-CH₂/Si-CH₃ bond ratio and defects after a CMP process of an insulating film in the embodiment of the present invention shown in Fig. 6;

Figs. 9A-9D are cross sectional views illustrating in order a process of forming a semiconductor device according to another embodiment of the present invention; and

20 Fig. 10 is a graph showing a relationship between Si-CH₂/Si-CH₃ bond ratio and yield of an insulating film in the embodiment of the present invention shown in Figs. 9A-9D.

Description of a Preferred Embodiment

25 With reference to the drawings, embodiments of the present invention will now be described.

[Embodiment 1]

30 In this embodiment, an explanation will be made on a method of forming an insulating film according to the present

invention, that is, an SiOCH film having Si-CH₂ bond in the film, on a semiconductor substrate. Fig. 1 illustrates a schematic structure of a parallel plate electrode type plasma enhanced CVD apparatus which can be used for forming the 5 SiOCH film according to the present invention.

The apparatus shown in Fig. 1 comprises a processing chamber 17 within which film forming process is performed on a semiconductor substrate 11, and a susceptor 12 which is disposed in the processing chamber 17 and which functions as a 10 lower plate electrode. The susceptor 12 has a heater for heating a semiconductor substrate 11 placed on the susceptor 12 and for keeping the temperature of the semiconductor substrate 11 constant. The apparatus shown in Fig. 1 also comprises a transporting means (not shown in the drawing) for 15 carrying the semiconductor substrate 11 into the processing chamber 17 and for carrying the semiconductor substrate 11 out of the processing chamber 17. The apparatus shown in Fig. 1 further comprises an exhaust means 13 which keeps the pressure in the processing chamber 17 constant, a gas supply portion 14 which supplies a plurality of kinds of reaction gases 20 into the processing chamber 17, and a high frequency signal generator 15.

Within the processing chamber 17, there are provided an upper plate electrode 16 and the susceptor 12 as a lower plate 25 electrode in opposed dispositions. The upper plate electrode 16 is electrically coupled with the high frequency signal generator 15 mentioned above. Also, the susceptor 12 has the heater mentioned above which is built therein. The high frequency signal generator 15 generates and supplies a high 30 frequency power (RF power) signal, which has a predetermined

frequency and a predetermined high frequency power, between the upper plate electrode 16 and the susceptor 12 as the lower plate electrode.

When the SiOCH film is formed by using the plasma enhanced CVD apparatus which has the above-mentioned structure, the semiconductor substrate 11 placed on the susceptor 12 is heated to a desired temperature by the heater built in the susceptor 12. Also, predetermined kinds of reaction gases are supplied into the processing chamber 17 at predetermined flow rates, thereby a desired gas atmosphere and a desired processing pressure are realized within the processing chamber 17. A high frequency RF power signal having a desired frequency is applied between the upper plate electrode 16 and the susceptor 12, and plasma of reaction gases is produced within the processing chamber 17. Thereby, the SiOCH film is formed on the semiconductor substrate 11.

Next, a detailed explanation will be made on a method of forming the SiOCH film by using the above-mentioned plasma enhanced CVD apparatus. In this embodiment, trimethyl silane and oxygen were used as source gases to form the SiOCH film. In a typical film forming condition, a film forming temperature is 350°C, and source gases comprise trimethyl silane at a flow rate of 1100 sccm and oxygen (O₂) at a flow rate of 450 sccm. Also, an RF power is 700W, and a pressure is 4.5Torr.

Also, the inventors formed SiOCH films having various film characteristics, by changing these film forming conditions, i.e., RF power, gas flow rate, temperature and pressure, and measured the film characteristics. As a result thereof, the inventors found that there are close relationships between the

-10-

proportion of Si-CH₂ bond (1360cm⁻¹) to Si-CH₃ bond (1270cm⁻¹) in each film in Fourier Transform Infrared

Spectroscopy (FTIR) spectrum and film characteristics. That is, in a film which has Si-CH₂ bond, as the Si-CH₂ bond / Si-

5 CH₃ bond ratio becomes higher, ashing tolerance and adhesion become improved, and also dielectric constant becomes larger. On the other hand, as the Si-CH₂ bond / Si-CH₃ bond ratio becomes lower, a change in each of these parameters shows an opposite tendency.

10 Figs. 2A through 2C show peak curves of Si-CH₂ in FTIR spectra, peak curves of Si-CH₃ in FTIR spectra, and ratios of Si-CH₂ to Si-CH₃ calculated from these peak curves, respectively, concerning SiOCH films formed in various conditions in which RF powers are changed from 560W through 15 630W, 700W, 770W and 840W.

Fig. 2A shows peaks of Si-CH₂ bond having a wave number of 1360cm⁻¹ in FTIR spectra. From Fig. 2A, it can be seen that, as the RF power becomes large, Si-CH₂ bond increases.

20 Fig. 2B shows peaks of SiCH₃ bond having a wave number of 1270cm⁻¹ in FTIR spectra. From Fig. 2B, it can be seen that, as the RF power becomes large, Si-CH₃ bond decreases.

25 Fig. 2C is a table showing a result of ratios of Si-CH₂ to Si-CH₃ calculated from these peak curves. From Fig. 2C, it can be seen that, as the RF power increases, the ratios of Si-CH₂ bond to Si-CH₃ bond increase.

30 With respect to the samples of SiOCH films obtained in this way and having the ratios of Si-CH₂ bond to Si-CH₃ bond shown in Fig. 2C, ashing tolerance and adhesion to the SiO₂

film (CAP-SiO₂ film) which is formed as the upper layer on the SiOCH film were examined.

With respect to the ashing tolerance, a parallel plate type O₂ ashing apparatus was used, and ashing process was 5 performed in the following conditions. That is, flow rate of ashing gas, O₂, was 500 sccm, RF power was 1000W, process time was 60 seconds, and process temperature was 100°C. Fig. 3 shows: relative dielectric constant of SiOCH film before the ashing process in ordinate of left side; and increase in relative 10 dielectric constant of SiOCH film after the ashing process in ordinate of right side; with respect to the ratios of Si-CH₂ to Si-CH₃ shown by the abscissa. From Fig. 3, it can be seen that, as Si-CH₂ bond increases, ashing tolerance is improved. On the other hand, as the Si-CH₃ group decreases, the relative 15 dielectric constant increases. It can be seen that, in a range of Si-CH₂/Si-CH₃ ratio from 0.03 to 0.05, relative dielectric constant is 3 or lower and increase in the relative dielectric constant caused by ashing becomes 0.1 or lower. That is, in this range, it is possible to keep the relative dielectric constant 20 of SiOCH film equal to or lower than 3.1, even after performing the ashing process.

Fig. 4 shows a relationship between an adhesion of a CAP-SiO₂ film and an Si-CH₂/Si-CH₃ ratio, measured by using a four point bending method. From Fig. 4, it can be seen that, 25 when the Si-CH₂/Si-CH₃ ratio becomes high, the adhesion becomes improved. This is because, when the Si-CH₂/Si-CH₃ ratio becomes high, CH₃ groups which are hydrophobic groups decrease, and Si-CH₂ bonds hide in -Si-O- network, so that affinity for SiO₂ film increases. Therefore, from the point of 30 view of adhesion, it is preferable that the Si-CH₂ bond/Si-CH₃

bond ratio is high. However, when the Si-CH₂ bond/Si-CH₃ bond ratio becomes high, dielectric constant also increases. Therefore, it is preferable that the Si-CH₂ bond/Si-CH₃ bond ratio is in a range from 0.03 to 0.05.

5 In the above, an explanation was made on an example in which RF power was changed to change Si-CH₂ bond/Si-CH₃ bond ratio. Fig. 5 shows relationships between various parameters in forming the film and Si-CH₂ bond/Si-CH₃ bond ratio. From Fig. 5, it can be seen that, when O₂ flow rate is
10 relatively low, when a pressure is relatively low and when a temperature is relatively high, the Si-CH₂ bond/Si-CH₃ bond ratio becomes high. Therefore, by optimizing these parameters, it is possible to form a SiOCH film having the Si-CH₂ bond/Si-CH₃ bond ratio of 0.03-0.05.

15 By using the method mentioned above, it is possible to form an insulating film according to the present invention, that is, an SiOCH film having Si-CH₂ bond within the film. In this case, it is preferable that the Si-CH₂ bond/Si-CH₃ bond ratio is in a range between 0.03 and 0.05, and, by using the ratio in this
20 range, it is possible to keep the relative dielectric constant of the SiOCH film equal to or lower than 3.1 even after performing ashing.

Also, in the above, an explanation was made on a method of forming the SiOCH film by using a plasma enhanced CVD apparatus. However, by using methylsilsesquioxane (MSQ) formed by coating and by controlling base material, it is also possible to form an SiOCH film which has Si-CH₂ bond within the film, in which the Si-CH₂ bond/Si-CH₃ bond ratio is in a range between 0.03 and 0.05, and in which the relative
30 dielectric constant of the SiOCH film can be kept equal to or

lower than 3.1 even after ashing.

[Embodiment 2]

An explanation will now be made on a second 5 embodiment of the present invention. In the second embodiment, an SiOCH film according to the present invention is applied to a single damascene wiring structure.

Fig. 6 is a cross sectional view illustrating a 10 semiconductor device according to the second embodiment of the present invention. In Fig. 6, reference numeral 81 designates a ground insulating film formed on a semiconductor substrate (not shown in the drawing) on which semiconductor elements such as transistors, capacitors and the like (not shown in the drawing) are formed. On the ground insulating film 81, 15 a first interlayer insulating film is formed which comprises, from a lower layer to an upper layer, a first SiCNH film 82, a first SiOCH film 83, and a first SiO₂ film (i.e., first CAP-SiO₂ film) 84. The first SiCNH film 82 is formed as an anti metal diffusion insulating film for preventing diffusion of metal such 20 as Cu and the like, and has a film thickness of 50nm. The first SiOCH film 83 is a film which has a film thickness of 250nm, and which has Si-CH₂ bond therein and Si-CH₂ bond/Si-CH₃ bond ratio thereof is preferably 0.03-0.05. The first SiO₂ film 84 has a film thickness of 100nm.

25 In a wiring trench formed in the first interlayer insulating film, a first Cu wiring conductor 87 is formed via a first Ta/TaN film 86. The first Ta/TaN film 86 is formed as a barrier metal layer and has a film thickness of 30nm. The first Cu wiring conductor 87 is a first metal wiring conductor 30 which comprises Cu as Cu containing metal.

On the upper surface of the first SiO₂ film 84 and the first Cu wiring conductor 87, a second interlayer insulating film is formed which comprises, from a lower layer to an upper layer, a second SiCNH film 88, a second SiOCH film 89, and a second 5 SiO₂ film (i.e., second CAP-SiO₂ film) 90. The second SiCNH film 88 is formed as an anti metal diffusion insulating film for avoiding diffusion of metal, and has a film thickness of 50nm. The second SiOCH film 89 is a film which has a film thickness of 250nm, and which has Si-CH₂ bond therein and Si-CH₂ 10 bond/Si-CH₃ bond ratio thereof is preferably 0.03-0.05. The second SiO₂ film 90 has a film thickness of 100nm.

In the second interlayer insulating film, there is formed an opening (i.e., a via) which penetrates through the second interlayer insulating film and which reaches the first Cu wiring conductor 87, that is, the lower layer metal wiring conductor. 15 In the opening, there is formed a Cu plug 93 via a second Ta/TaN film 92. The second Ta/TaN film 92 is formed as a barrier metal layer and has a film thickness of 30nm. The Cu plug 93 is a metal plug which comprises Cu as Cu containing 20 metal.

On the upper surface of the second SiO₂ film 90 and the Cu plug 93, a third interlayer insulating film is formed which comprises, from a lower layer to an upper layer, a third SiCNH film 95, a third SiOCH film 96, and a third SiO₂ film (i.e., third 25 CAP-SiO₂ film) 97. The third SiCNH film 95 is formed as an anti metal diffusion insulating film for avoiding diffusion of metal, and has a film thickness of 50nm. The third SiOCH film 96 is a film which has a film thickness of 250nm, and which has Si-CH₂ bond therein and Si-CH₂ bond/Si-CH₃ bond 30 ratio thereof is preferably 0.03-0.05. The third SiO₂ film 97

has a film thickness of 100nm.

In the third interlayer insulating film, there is formed a wiring trench which penetrates through the third interlayer insulating film and which reaches the Cu plug 93 of the lower 5 layer. In the wiring trench, there is formed a second Cu wiring conductor 99 via a third Ta/TaN film 98. The third Ta/TaN film 98 is formed as a barrier metal layer and has a film thickness of 30nm. The second Cu wiring conductor 99 is a second metal wiring conductor which comprises Cu as Cu 10 containing metal.

Next, an explanation will be made on a method of manufacturing a single damascene wiring structure shown in Fig. 6 to which SiOCH films according to the present invention are applied. Figs. 7A-7D are cross sectional views each 15 illustrating, in order of process steps, a workpiece of a semiconductor device according to the second embodiment obtained during a process of manufacturing thereof.

With reference to Fig. 7A, first, on a ground insulating film 81 formed on a semiconductor substrate (not shown in the drawing) on which semiconductor elements such as transistors, capacitors and the like (not shown in the drawing) are formed, a first SiCNH film 82 is formed by using a plasma enhanced CVD method to a film thickness of 50nm. Then, also by using a plasma enhanced CVD method, a first SiOCH film 83 is formed 20 to a film thickness of 250nm. The first SiOCH film 83 has Si-CH₂ bond therein and Si-CH₂ bond/Si-CH₃ bond ratio thereof is preferably 0.03-0.05. Thereafter, the first SiO₂ film (i.e., first CAP-SiO₂ film) 84 is formed by using a plasma enhanced 25 CVD method to a film thickness of 100nm. In this process, process temperature is 200-450°C, N₂O gas flow rate is 100- 30

6000 sccm, SiH₄ gas flow rate is 10-1000 sccm, process pressure is 1-20Torr, and RF power is 50-500W. It is also possible to form the first SiO₂ film 84 in the same vacuum chamber as that used for forming the first SiOCH film 83, continuously after

5 forming the first SiOCH film 83. By the process steps mentioned above, the first interlayer insulating film comprising three layers is formed which comprises, from a lower layer to an upper layer, the first SiCNH film 82, the first SiOCH film 83, and the first SiO₂ film 84.

10 Next, by using a photolithography technology and a dry etching technology, a wiring trench 85 is formed which penetrates through the first SiO₂ film 84, the first SiOCH film 83 and the first SiCNH film 82, as clearly shown in Fig. 7A.

15 With reference to Fig. 7B, on an exposed inside wall of the wiring trench 85 and on the upper surface of the first SiO₂ film 84, a Ta/TaN film 86 is formed to a film thickness of 30nm. On the Ta/TaN film 86, a Cu layer is formed to a film thickness of 100nm by using a sputtering method. The Cu layer is used as a cathode side ground layer for an electrolytic plating method. Thereafter, the wiring trench 85 is filled with Cu by using an electrolytic plating method. Further, a heat treatment is performed thereafter at a temperature of 100-400°C for crystallization. Then, the Cu layer and the Ta/TaN film 86 on the first SiO₂ insulating film 84 are removed by a

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25 CMP method. Thereby, the first Cu wiring conductor 87 is formed within the wiring trench 85, as clearly shown in Fig. 7B.

With reference to Fig. 7C, a second interlayer insulating film is formed on the workpiece obtained by the process mentioned above. That is, by using a procedure similar to that mentioned above, a second SiCNH film 88 is formed to a film

thickness of 50nm. Then, by using a plasma enhanced CVD method, a second SiOCH film 89 is formed to a film thickness of 250nm which has Si-CH₂ bond therein and Si-CH₂ bond/Si-CH₃ bond ratio thereof is preferably 0.03-0.05. Further, a 5 second SiO₂ film (a second CAP-SiO₂ film) 90 is formed to a film thickness of 100nm.

By using a photolithography technology and a dry etching technology, there is formed an opening (i.e., a via) 91 which penetrates through the second interlayer insulating film 10 and which reaches the first Cu wiring conductor 87, as clearly shown in Fig. 7C.

With reference to Fig. 7D, on an inside wall of the opening 91 and on the upper surface of the second SiO₂ film 90, a second Ta/TaN film 92 is formed to a film thickness of 30nm. 15 On the second Ta/TaN film 92, a Cu layer is formed to a film thickness of 100nm by using a sputtering method. The Cu layer is used as a cathode side ground layer for an electrolytic plating method. Thereafter, the opening 91 is filled with Cu by using an electrolytic plating method. Further, a heat 20 treatment is performed at a temperature of 100-400°C for crystallization. Then, the Cu layer and the Ta/TaN film 92 on the second SiO₂ insulating film 90 are removed by a CMP method. Thereby, a Cu plug 93 is formed within the opening 91 as a metal plug, as clearly shown in Fig. 7D.

25 Thereafter, referring back again to Fig. 6, a third interlayer insulating film is formed on the workpiece obtained as mentioned above. That is, by using a procedure similar to that mentioned above, a third SiCNH film 95 is formed to a film thickness of 50nm. Then, by using a plasma enhanced CVD 30 method, a third SiOCH film 96 is formed to a film thickness of

250nm which has Si-CH₂ bond therein and Si-CH₂ bond/Si-CH₃ bond ratio thereof is preferably 0.03-0.05. Further, a third SiO₂ film (a third CAP-SiO₂ film) 97 is formed to a film thickness of 100nm.

5 By using a photolithography technology and a dry etching technology, there is formed a wiring trench which penetrates through the third interlayer insulating film and which connects at a portion thereof to the Cu plug 93 of lower layer. Next, in a manner similar to the method mentioned
10 above, on an inside wall of the wiring trench and on the upper surface of the third SiO₂ film 97, a third Ta/TaN film 98 is formed, and on the third Ta/TaN film 98, a Cu layer is formed. The Cu layer is used as a cathode side ground layer for an electrolytic plating method. Thereafter, the wiring trench is
15 filled with Cu by using an electrolytic plating method. Further, a heat treatment is performed at a temperature of 100-400°C for crystallization. Then, the Cu layer and the Ta/TaN film 98 on the third SiO₂ insulating film 97 are removed by a CMP method. Thereby, a second Cu wiring
20 conductor 99 is formed within the wiring trench. By the process mentioned above, the two layer wiring structure having a single damascene structure was formed.

Fig. 8 shows a relationship between a number of defects of Cu portion after performing a CMP process and a film
25 composition, i.e., Si-CH₂/Si-CH₃ ratio, of a SiOCH film which is used as an interlayer insulating film, when the above-mentioned Cu wiring conductor is formed. From Fig. 8, it can be seen that, as the proportion of Si-CH₂ bond to Si-CH₃ bond becomes large, the number of CMP defects once decreases, and,
30 as the proportion of Si-CH₂ bond further becomes large, the

number of CMP defects increases again. This is because, as shown in Fig. 4 before, when the proportion of Si-CH₂ bond becomes large, the proportion of Si-CH₃ bond which deteriorates adhesion decreases, and adhesion between CAP-

5 SiO₂ film and SiOCH film is improved, so that delamination of CAP-SiO₂ film caused by CMP process decreases and defects of Cu decreases. When the proportion of Si-CH₂ bond further increases, -CH₂- bond is introduced into -O-Si-O- bond, so that the film strength deteriorates and the number of defects again 10 increases. Therefore, in order to keep the number of defects small, it is preferable that the Si-CH₂ bond/Si-CH₃ bond ratio of the SiOCH film is in a range from 0.03 to 0.05. When the Si-CH₂ bond/Si-CH₃ bond ratio is in this range, it is also 15 possible to suppress disadvantages such as the delamination of CAP-SiO₂ film when fabricating the device and the like can be avoided.

[Embodiment 3]

An explanation will now be made on a third embodiment 20 of the present invention. In the third embodiment, a dual damascene wiring structure is formed by using an interlayer insulating film according to the present invention.

Figs. 9A-9D are cross sectional views each illustrating, in order of process steps, a workpiece of a semiconductor device 25 according to the third embodiment of the present invention obtained during a process of manufacturing thereof.

With reference to Fig. 9A, first, on a ground insulating film 81 formed on a semiconductor substrate (not shown in the drawing) on which semiconductor elements such as transistors, 30 capacitors and the like (not shown in the drawing) are formed, a

first interlayer insulating film comprising three layers designated by reference numerals 82, 83 and 84 are formed in this order from a lower layer to an upper layer, by using process steps similar to those mentioned above with respect to the

5 second embodiment. That is, as an anti metal diffusion insulating film for preventing diffusion of metal, a first SiCNH film 82 is formed to a film thickness of 50nm. Then, a first SiOCH film 83 is formed to a film thickness of 250nm. Thereafter, the first SiO₂ film (i.e., first CAP-SiO₂ film) 84 is
10 formed to a film thickness of 100nm.

Next, within a wiring trench formed such that the wiring trench penetrates through the first interlayer insulating film, a first Cu wiring conductor 87 which is a first metal wiring conductor is formed via a first barrier metal Ta/TaN film 86.

15 With reference to Fig. 9B, a second interlayer insulating film comprising three layers 88, 89 and 90 is formed on the SiO₂ film 84 and the upper surface of the first Cu wiring conductor 87. That is, a second SiCNH film 88 as an anti metal diffusion insulating film is formed to a film thickness of
20 50nm. Then, by using a plasma enhanced CVD method, a second SiOCH film 89 is formed to a film thickness of 500nm which has Si-CH₂ bond therein and Si-CH₂ bond/Si-CH₃ bond ratio thereof is preferably 0.03-0.05. Thereafter, a second SiO₂ film (a second CAP-SiO₂ film) 90 is formed to a film thickness
25 of 100nm.

By using a photolithography technology and a dry etching technology, there is formed an opening 91 from the surface of the second SiO₂ film 90 until it reaches the second SiCNH film 88, as clearly shown in Fig. 9B.

30 Next, with reference to Fig. 9C, by using a

photolithography technology and a dry etching technology, there is formed a wiring trench 94 in an area including the opening 91. Also, a portion of the SiCNH film 88 at the bottom portion of the opening 91 is opened, such that the opening 91 5 reaches the upper surface of the first Cu wiring conductor 87 which becomes a lower layer metal wiring conductor. In this case, the wiring trench 94 is formed halfway through the thickness of the second SiOCH film 89.

Next, on an inside wall of the opening 91 and the wiring trench 94 and on the upper surface of the second SiO₂ film 90, a second Ta/TaN film 100 is formed as a barrier metal layer to a film thickness of 30nm. On the second Ta/TaN film 100, a Cu layer is formed to a film thickness of 100nm by using a sputtering method. The Cu layer is used as a Cu containing metal which becomes a cathode side ground layer for an electrolytic plating method. Thereafter, the opening 91 and the wiring trench are filled with Cu as the Cu containing metal by using an electrolytic plating method. Further, a heat treatment is performed at a temperature of 100-400°C for 15 crystallization. Then, the Cu layer and the Ta/TaN film on the second SiO₂ insulating film 90 are removed by a CMP method. Thereby, Cu plug and second Cu wiring conductor (designated by a common reference numeral 101) are simultaneously formed as metal plug and second metal wiring conductor. In 20 this way, a two layer wiring conductor formed by Cu and having a dual damascene structure is formed, as clearly shown in Fig. 25 9D.

Fig. 10 shows a relationship between the yield from 1,000,000 via chains of two layer Cu wiring conductors and the 30 Si-CH₂/Si-CH₃ ratio of an SiOCH film which is used as an

interlayer insulating film, when the Cu two layer wiring conductors are formed in accordance with the above-mentioned dual damascene method. From Fig. 10, it can be seen that, as the Si-CH₂ bond/Si-CH₃ bond ratio becomes small, the yield 5 becomes small. This is because, in such case, ashing tolerance deteriorates, and, therefore, outgassing of moisture and the like from the side surface of via forming portion increases, so that via is not completely filled with Cu and the like. On the other hand, when the Si-CH₂ bond/Si-CH₃ bond ratio is too high, the 10 yield becomes small. It is considered that when the Si-CH₂ bond/Si-CH₃ bond ratio is too high, the film strength deteriorates so that the interlayer insulating film is damaged when CMP process is performed. Therefore, in order to obtain high yield, it is preferable that the Si-CH₂ bond/Si-CH₃ bond 15 ratio of the SiOCH film is in a range from 0.03 to 0.05.

In the above description, an explanation was made on a method of forming a dual damascene wiring structure, by using a via-first technology in which a wiring trench is formed after forming an opening (i.e., a via). However, the present 20 invention is not limited to such method. For example, the present invention can also be applied to a trench-first method in which an opening (i.e., a via) is formed after forming a wiring trench. It is also possible to use a middle-first method in which an SiCH film or an SiCNH film which functions as an 25 etching stopper layer is inserted into the second SiOCH film, and, after processing the etching stopper layer first, a wiring trench and a via opening are simultaneously formed.

Further, in the second and third embodiments mentioned above, the Cu containing metal which constitutes the metal 30 wiring conductor (metal wire) and the metal plug was Cu, that

is, the metal wiring conductor was a Cu wiring conductor and the metal plug was a Cu plug. However, the Cu containing metal can be a Cu containing metal which contains, in addition to Cu, at least one of: Si, Al, Ag, W, Mg, Be, Zn, Pd, Cd, Au, Hg, 5 Pt, Zr, Ti, Sn, Ni and Fe. In case the Cu containing metal contains these materials, it is possible to further improve the life of wiring conductors in a semiconductor device which has the structure according to the present invention.

According to the above-mentioned constitution of the 10 present invention, an insulating film is provided which is a carbon containing oxide silicon (SiOCH) film and which has - Si-CH₂- bond in the film. Therefore, it becomes possible to improve ashing tolerance, without causing a rise in the dielectric constant of the interlayer insulating film which especially requires low dielectric constant. Also, as described 15 before with reference to Fig. 4, it is possible to improve adhesion to the CAP-SiO₂ film.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, 20 one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative sense rather than a restrictive sense, 25 and all such modifications are to be included within the scope of the present invention. Therefore, it is intended that this invention encompasses all of the variations and modifications as falling within the scope of the appended claims.